UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/618,462	07/11/2003	Guangming Yin	BP1817CON1	3869

34399 7590 06/01/2005

GARLICK HARRISON & MARKISON LLP
P.O. BOX 160727
AUSTIN, TX 78716-0727

EXAMINER	
NGUYEN, PATRICIA T	

ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 06/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/618,462	YIN ET AL.	
	Examiner	Art Unit	
	Patricia T. Nguyen	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *30-58* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *35-42* is/are allowed.

6)☒ Claim(s) *30,32-34 and 43-58* is/are rejected.

7)☒ Claim(s) *31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/4/05, 11/30/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 30, 32, and 33 are rejected under 35 U.S.C. 102(b) as being anticipated by Leung et al., A 3-V 45 mW CMOS Differential Bandpass Amplifier For GSM Receivers, 1998 IEEE (0-7803-4455-3/98).

Fig. 5 of Leung et al. discloses an amplifier comprising: transistor Md can be read as a current source; transistor M1+ can be read as a first differential transistor having a source, gate, and drain, wherein the source of the first differential transistor is coupled to the current source; transistor M1- can be read as a second differential transistor having a source, gate, and drain, wherein the source of the second differential transistor is coupled to the current source; resistor Ro connected to transistor M1+ can be read as a first output resistor having positive and negative ends, wherein the negative end of the first output resistor is coupled to the drain of the first differential transistor (M1+); resistor Ro connected to transistor M1- can be read as a second output resistor having positive and negative ends, wherein the negative end of the second output resistor is coupled to the drain of the second differential transistor (M1-);

Inductor Lo connected to the first output resistor Ro connected to transistor M1+ can be read as a first shunt peaking inductor having positive and negative ends, wherein the negative end of the first shunt peaking inductor is coupled to the positive end of the first output resistor; and inductor Lo connected to the second output resistor Ro connected to transistor M1- can be read as a second shunt peaking inductor having positive and negative ends, wherein the negative end of the second shunt peaking inductor is coupled to the positive end of the second output resistor.

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 30, 32, and 33 are rejected under 35 U.S.C. 102(e) as being anticipated by Momtaz et al., U.S. Patent # 6,864,558 B2.

Fig. 2 of Momtaz et al. discloses an amplifier comprising: transistor 212 can be read as a current source; transistor 202 can be read as a first differential transistor having a source, gate, and drain, wherein the source of the first differential transistor is coupled to the current source; transistor 204 can be read as a second differential transistor having a source, gate, and drain, wherein the source of the second differential transistor is coupled to the current source; resistor 206 can be read as a first output resistor having positive and negative ends, wherein the negative end of resistor 206 is coupled to the drain of the first differential transistor (202); resistor 207 can be read as a

second output resistor having positive and negative ends, wherein the negative end of resistor 207 is coupled to the drain of the second differential transistor (204); Inductor 208 can be read as a first shunt peaking inductor having positive and negative ends, wherein the negative end of the first shunt peaking inductor is coupled to the positive end of the first output resistor (206); and inductor 209 can be read as a second shunt peaking inductor having positive and negative ends, wherein the negative end of the second shunt peaking inductor is coupled to the positive end of the second output resistor (207).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 34, 43-58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leung et al., A 3-V 45 mW CMOS Differential Bandpass Amplifier For GSM Receivers, 1998 IEEE (0-7803-4455-3/98) in view of Ryan et al., U.S. Patent # 6,414,558 B1.

Regarding claim 34, although Leung et al. does not show that the first and second differential transistors and the current source transistor comprise PMOS transistors it would have been obvious at the time the invention was made to a person having ordinary skill in the art to reverse the transistors from NMOS to PMOS in the

absence of unexpected results since this is a well known practice in the art and this is a matter of design choice.

Regarding claims 43-58, although Leung et al. does not have multistage differential amplifier, Ryan et al. teaches in Fig. 3A a multistage differential amplifier, therefore it would have been obvious at the time the invention was made to a person having ordinary skill in the art to use the differential amplifier of Leung et al. in the circuit of Ryan et al. in order to have an optimum performance for the circuit.

Claim 34 is rejected under 35 U.S.C. 103(a) as being unpatentable over Momtaz et al., U.S. Patent # 6,864,558 B2 in view of Ryan et al., U.S. Patent # 6,414,558 B1.

Regarding claim 34, although Momtaz et al. does not show that the first and second differential transistors and the current source transistor comprise PMOS transistors it would have been obvious at the time the invention was made to a person having ordinary skill in the art to reverse the transistors from NMOS to PMOS in the absence of unexpected results since this is a well known practice in the art and this is a matter of design choice.

Allowable Subject Matter

Claim 31 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 35-42 are allowed.

The following is a statement of reasons for the indication of allowable subject matter: prior art does not teach nor render obvious an amplifier that has, in combination with other limitations, a first miller capacitance cancellation capacitor having positive and negative ends, wherein the positive end of the first miller capacitance cancellation capacitor is coupled to the drain of the second differential transistor, and wherein the negative end of the first miller capacitance cancellation capacitor is coupled to the gate of the first differential transistor; and a second miller capacitance cancellation capacitor having positive and negative ends, wherein the positive end of the second miller capacitance cancellation capacitor is coupled to the drain of the first differential transistor, and wherein the negative end of the second miller capacitance cancellation capacitor is coupled to the gate of the second differential transistor.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. U.S. Patent # 6,774,721 B1 contain some limitations of the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Patricia T. Nguyen whose telephone number is (703) 308-1927. The examiner can normally be reached on 6:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on 703-309-4940. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PTN
May 24, 2005

Patricia Nguyen

PATRICIA NGUYEN
PRIMARY EXAMINER